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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,118	11/27/2001	Chuan-cheng Cheng	01-695/LSI1P184	5362

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,118	CHENG ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 37 CFR 1.114 claiming priority from U.S. Serial No. 09/996,118 filed on November 27, 2001 which papers have been placed of record in the file.

Continued Prosecution Application

The request filed on 01/02/2003 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/996,118 is acceptable and a RCE has been established. An action on the RCE follows.

Drawings

The drawings filed on November 27, 2001 have been objected to by the drafts person for the reasons set out in the enclosed PTO-948.

Appropriate correction is required.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 01/02 /2003 . Therefore claims 12 to 21 as recited in the preliminary amendment are currently pending in the Application.

Claims 6 and 9-11 were cancelled by the preliminary amendment.

Claim 7 was cancelled by the amendment after Final that was not entered but is being cancelled by the following Examiner's amendment.

Examiner's Amendment.

Cancel claim 7 (that was cancelled in the non-entered amendment after Final) and treated by Applicants' as being cancelled in their preliminary amendment of 1/2/03.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13 the phrase "in a tone reversed from that used for patterning and etching the dielectric" renders the claim indefinite because it is not clear what the applicant's intend to include or exclude by the above recitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 to 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McTerr (U.S. Patent No. 5,939, 788, herein after McTerr) and Robinson et al. (U.S> Patent No. 6,054,172 herein after Robinson) both previously applied for reasons previously set out and those set out below.

With respect to claim 12, McTerr describes a method for fabricating a low resistance interconnect line in an integrated circuit, the method comprising the steps of : forming a dielectric layer on a substrate of an integrated circuit (McTerr figure 4 layer # 7 over 10) patterning and etching the dielectric layer to form a trench, (McTerr fig. 5) wherein the patterning is performed using a first photomask; (McTerr col. 17 lines 45-46) filling the trench in the dielectric layer with copper; (McTerr, fig. 3 # 3, col. 17 lines 63-65) polishing the copper and the dielectric to form a first planarized surface comprising a top polished surface of the copper and a top polished surface of the dielectric, (McTerr col. 20 , lines 40-47) wherein the top polished surface of the copper and the trench define a lower conductive metal portion of the interconnect line, the lower conductive metal portion comprising copper; (McTerr figs. 3, 6 etc.) depositing an aluminum layer on at least a portion of the top polished surface of the dielectric and at least a portion of the top polished surface of the copper of the first planarized surface; (McTerr figs. 14 and col. 22 lines 45-50) patterning and etching the aluminum to define an upper conductive metal portion of the interconnect line, wherein the upper conductive metal portion is further defined so that the aluminum overlies the lower conductive metal portion. (McTerr figure 14, patterning and palanrization) .

McTerr does not specifically mention an etching step.

However, Robinson, in col. 8 lines 13-018 describes an etching step as part of of a patterning process to form a patterned aluminum layer that acts as a catalyst in preventing native oxide formation from the titanium containing material thus allowing the deposition of Copper layer with fewer impurities resulting in allow resistivity path through the titanium-containing and cooper layers with the IC, particularly in the interconnect structure of an IC where resistance to electrical current should be minimized.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Robison's etching step as part of the patterning step in McTerr's process steps to from a patterned aluminum layer that acts as catalyst in preventing native oxide formation from the titanium containing material allowing the deposition of Copper layer with fewer impurities resulting in a low resisitivity path through the titanium-containg and cooper layers within the IC, particularly in the interconnect structure of an IC where resistance to electrical current should be minimized. (Robinson col. 8 lines 10-28).

With respect to claim 13, to the extent understood, the method for fabricating low resistance interconnect lines as recited in claim 12 wherein the first photomask is used to pattern the aluminum layer to define the upper conductive metal portion of the interconnect in a tone reversed from that used for patterning and etching the dielectric. (McTerr figures 1 to 5, col. 18 lines 15-25 and claim 7).

With respect to claim 14 , McTerr describes the method for fabricating low resistance interconnect lines as recited in claim 12 wherein the low resistance interconnect comprises two layers of conductive metal over its length between a first

connection point and a second connection point in the integrated circuit, wherein the lower conductive metal layer comprises copper and the upper conductive metal layer comprises aluminum. (McTerr fig. 1 # 3, col. 17 line 52 and fig.2 # %, col. 18 lines 18-19).

With respect to claim 15 McTerr describes the method for fabricating low resistance interconnect lines as recited in claim 12 wherein the aluminum layer is deposited directly on the first planarized surface. (McTerr fig.4, col 18 line 9).

With respect to claim 16, McTerr describes the method for fabricating low resistance interconnect lines as recited in claim 12 further comprising, depositing a barrier layer directly on the first planarized surface. (McTerr fig. 4, col. 18 line 9).

With respect to claim 17, McTerr describes the method for fabricating low resistance Interconnect lines as recited in claim 16 wherein the aluminum layer is deposited directly on the barrier layer. (McTerr col. 18 lines 17-21).

With respect to claims 18-20 , McTerr describes the Cooper has a thickness within the range of 0.3 to 2.0 um and the aluminum ahs a thickness within the range of 0.5 microns to 3.0 um. (McTerr col.22 lines 60 100-800 Angstroms i.e. 0.01 to 0.08 um) and claim 26 cooper 100 –2000 angstroms thick i.e. 0.01 to .02 um). Therefore without a showing of criticality or unexpected results the recited range of thickness is obvious in view of previously described overlapping ranges.

Allowable Subject Matter

Claim 21 will be allowed if rewritten in independent form to include all the limitations of claims 12 and 20.

The following is a statement of reasons for the indication of allowable subject matter the prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitation of the dependent claims, in such manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in independent claims, which include :

A method for fabricating a low resistance interconnect line in an integrated circuit, the method comprising the steps of forming a dielectric layer on a substrate of an integrated circuit, patterning and etching the dielectric layer to form a trench., wherein the patterning is performed using a first photomask; filling the trench in the dielectric layer with copper; polishing the copper and the dielectric to form a first planarized surface comprising a top polished surface of the copper and a top polished surface of the dielectric, wherein the top polished surface of the copper and the trench define a lower conductive metal portion of the interconnect line, the lower conductive metal portion comprising copper; depositing an aluminum layer on at least a portion of the top polished surface of the dielectric and at least a portion of the top polished surface of the copper of the first planarized surface; and patterning and etching the aluminum to define an upper conductive metal portion of the interconnect line, wherein the upper conductive metal portion is further defined so that the aluminum overlies the lower conductive metal portion and wherein the copper has a thickness within the range of 0.3 to 2.0 ~tm and the aluminum has a thickness within the range of 0.5 to 3.0 ~tm and thickness of the copper and the thickness of the aluminum are adjusted so that the

completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 f2 per unit length.

The located prior art teaches /suggests low resistance but does not specify the resistance to be within the range of 0.012 to 0.008 f2 per unit length.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5584. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

March 28, 2003.

LONG PHAM
PRIMARY EXAMINER